Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A repeat circuit for use with an audio receive and reproduce device including:

a RAM connected to normally receive and store audio inputs applied to said device;

a manually operable input component; and

a control operable in response to a selected input from said component for inhibiting application of incoming audio inputs to said device and for instead applying audio inputs stored in said RAM as audio inputs to said device, the audio reproduced by said device being selectively delayed from incoming audio inputs by a time dependent on where in said RAM said control begins the applying of audio inputs to said device;

wherein said control is operable in response to a rate indication from said input component for controlling the rate at which said RAM is read out to apply audio inputs to said device, said RAM being read out to apply inputs to said device at a different rate than audio inputs are received to be stored in said RAM.

2. (original) A circuit as claimed in claim 1, wherein the location in said RAM at which the applying of audio inputs begins, and thus the delay between incoming audio inputs and reproductions, is controllable in response to selective operation of said component.

3. (original) A circuit as claimed in claim 2, wherein said delay is a function of at least one of the number of times said component is operated and the time said component is operated.

4. (original) A circuit as claimed in claim 2, wherein when said device is receiving inputs from said RAM, the circuit is in replay mode, and including an output element providing a

selected indication that said circuit is in said replay mode, said output element also providing an indication of said delay.

5. (original) A circuit as claimed in claim 4, wherein said output element is a selected display, and wherein said control causes said display to blink at a rate which is a function of said delay.

6. (original) A circuit as claimed in claim 1, wherein when said device is receiving inputs from said RAM, the circuit is in replay mode, and including a multicolor LED, the LED displaying one color for replay mode, and a second different color for normal mode with incoming audio inputs applied to the device.

7. (original) A circuit as claimed in claim 6, wherein said RAM is a wrap-around memory, the oldest audio input therein being written over when a new audio input is received and said RAM is full, and wherein said control inhibits writing over of audio inputs in said RAM in response to a selected input from said input component, the circuit being in storage mode when this occurs, and wherein said LED displays a third color when said circuit is in storage mode.

8. (original) A circuit as claimed in claim 1, wherein said RAM is a wrap-around memory, the oldest audio input therein being written over when a new audio input is received and said RAM is full, and wherein said control inhibits writing over of audio inputs in said RAM in response to a selected input from said input component, the circuit being in storage mode when this occurs, and wherein said control causes incoming audio inputs to be applied to said device when the circuit is in storage mode.

9. (original) A circuit as claimed in claim 8, wherein said control is operative when the circuit is in storage mode to cause at least selected portions of audio inputs stored in said RAM to be reproduced on said device in response to a selected input from said input component.

10. (original) A circuit as claimed in claim 9, wherein said selected input is said input component being manually operated for a selected time interval.

11. (original) A circuit as claimed in claim 1, wherein said device is a radio, and wherein said circuit is returned from replay mode to a normal mode with incoming audio inputs applied to said device when there is a station change on said radio.

12. (original) A circuit as claimed in claim 1, wherein said control processes audio inputs applied to said RAM.

13. (currently amended) A circuit as claimed in claim 1, wherein said component is operable to indicate a desired rate at which audio inputs are to be reproduced to said device~~; and, wherein said control is operable in response to a rate indication from said component for controlling the rate at which said RAM is read out to apply audio inputs to said device~~.

14. (original) A circuit as claimed in claim 13, wherein said component is operable in at least two different ways, said component being operated in a selected way to indicate a desired rate.

15. (original) A circuit as claimed in claim 1, wherein said control is operative in response to a selected input to set said circuit into an elimination mode, said control being operative when in elimination mode to store in said RAM a selected duration of audio inputs ahead of inputs received by said RAM, and is responsive, when in elimination mode, to a selected input from said component for skipping an audio duration in said RAM which is less than said selected duration, whereby audio during said audio duration is not reproduced at said device.

16. (original) A circuit as claimed in claim 15, wherein said audio duration is variable in response to variations in the selected input from said component.

17. (original) A circuit as claimed in claim 15, wherein said control is operative when in elimination mode to store said selected duration in said RAM before applying audio inputs from said RAM to said device.

18. (original) A circuit as claimed in claim 15, wherein said control is operative, when in elimination mode to apply audio inputs to said device from said RAM, said RAM being read out to apply inputs to said device at a slower rate than audio inputs are received to be stored in said RAM at any time said RAM is not storing at least said selected duration of audio inputs.

19. canceled.

20. canceled.

21. canceled.

22. canceled.

23. (currently amended) A method for repeating audio inputs which are normally applied to an audio receive and reproduce device including:

a) digitally storing said audio inputs in a RAM for a selected interval starting from the currently received input; ~~and~~

b) inhibiting reproduction of currently received audio inputs by said device and causing the reproduction by said device from inputs received from said RAM in response to a manually controlled user input, the audio reproduced by said device being selectively delayed from incoming audio inputs by a time dependent on where in said RAM said control begins the applying of audio inputs to said device;[[.]]

c) controlling a rate at which said RAM is read out to apply audio inputs to said device, said rate being different than an input rate at which said audio inputs are received to be stored in said RAM.

24. canceled.

25. canceled.

26. (currently amended) A repeat circuit for use with an audio receive and reproduce device including:

A RAM connected to normally receive and store audio inputs applied to said device, said RAM being a wrap-around memory, the oldest audio input therein being written over when a new audio input is received and said RAM is full;

a manually operable input component; and

a control operable in response to a selected input from said component for inhibiting application of incoming audio inputs to said device and for instead applying audio inputs stored in said RAM as audio inputs to said device, said control ~~inhibiting~~ also operable to inhibit writing over of audio inputs in said RAM in response to a selected input from said input component, ~~the circuit being in storage mode when this occurs,~~ and ~~wherein said control causes~~ to cause said incoming audio inputs to be applied to said device when the circuit is in ~~storage~~ this mode;

wherein said control is also operable in response to a rate indication from said input component for controlling the rate at which said RAM is read out to apply audio inputs to said device, said RAM being read out to apply inputs to said device at a different rate than audio inputs are received to be stored in said RAM.

27. (original) A circuit as claimed in claim 26, wherein said control is operative when the circuit is in storage mode to cause at least selected portions of audio inputs stored in said RAM to be reproduced on said device in response to a selected input from said input component.

28. (currently amended) A repeat circuit for use with an audio receive and reproduce device including:

a RAM connected to normally receive and store audio inputs applied to said device;

a manually operable input component, said component being operable to indicate a desired rate at which audio inputs are to be reproduced to said device; and

a control operable in response to a selected input from said component for inhibiting application of incoming audio inputs to said device and for instead applying audio inputs stored in said RAM as audio inputs to said device, said control being operable in response to a rate

indication from said component for controlling the rate at which said RAM is read out to apply audio inputs to said device;

wherein the rate at which said RAM is read out is different than an input rate at which said audio inputs are received to be stored.

29. (newly added) The repeat circuit as claimed in claim 28, wherein the rate at which said RAM is read out is faster than the input rate at which said audio inputs are received to be stored in said RAM.

30. (newly added) The repeat circuit as claimed in claim 28, wherein the rate at which said RAM is read out is slower than the input rate at which said audio inputs are received to be stored in said RAM.

31. (newly added) The method as claimed in claim 23, further comprising a step of indicating a desired rate of playback of said audio inputs from said RAM.

32. (newly added) The method as claimed in claim 23, wherein said rate is slower than said input rate.

33. (newly added) The method as claimed in claim 23, wherein said rate is faster than said input rate.

34. (newly added) The repeat circuit as claimed in claim 1, wherein said rate at which said RAM is read out is faster than said different rate at which said audio inputs are received to be stored in said RAM.

35. (newly added) The repeat circuit as claimed in claim 1, wherein said rate at which said RAM is read out is slower than said different rate at which said audio inputs are received to be stored in said RAM.